**Report requirements for the project:**

**Cover page**: Name, course, semester, Year,  Project title:

1.       Describe the assignment.

2.       Describe the control unit design.

a) How instructions are decoded and the ALUSel and ShiftSel encoded

b) Whether the control circuit is FSM or Clock counter+ decoder+ Combination

   Number of states and the state graph

   Boolean expressions per control signals per cycle per instruction for the latter case.

3.       Hierarchy of  Verilog modules

4.       Waveforms: justification of selected inputs/outputs for verification. Screen shots.

5.       Explain the testbench. Proof you were able to verify operation in a comprehensive way. Screen shots.

6.       Cycle calculation. Performance analysis:  T= IC x CPI x Cycle.

7.       Concluding remarks. Analysis of the instruction set (if any thoughts).

8.       Appendix:  Copy of  .v files